MIC2810

Digital Power Management IC 2MHz, 600mA DC/DC w/Dual 300mA/300mA Low V_{IN} LDOs

General Description

The MIC2810 is a high performance power management IC, integrating a 2MHz DC/DC switcher with two 300mA LDOs. The MIC2810 features a *LOWQ*® mode, reducing the total current draw while in this mode to less than 30µA. In *LOWQ*® mode, the output noise of the DC/DC converter is 53µV_{RMS}, significantly lower than other converters that use a PFM light load mode that can interfere with sensitive RF circuitry.

The MIC2810 is a µCap design, operating with very small ceramic output capacitors and inductors for stability, therefore, reducing required board space and component cost. It is available with fixed output voltages in a 16-pin 3mm x 3mm MLF® leadless package.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- 2MHz DC/DC converter and two LDOs
- Integrated power-on reset (OR function for all outputs)
  - Adjustable delay time
- *LOWQ*® mode
  - 30µA Total I_Q when in *LOWQ*® mode
- Tiny 16-pin 3mm x 3mm MLF® package
- Thermal shutdown protection
- Current limit protection

DC/DC Converter

- 2.7V to 5.5V input voltage range
- Output current to 600mA in PWM mode
- *LOWQ*® Mode: NO NOISE light load mode
  - 53µV_{RMS} Output noise in *LOWQ*® mode
- 2MHz PWM operation in normal mode

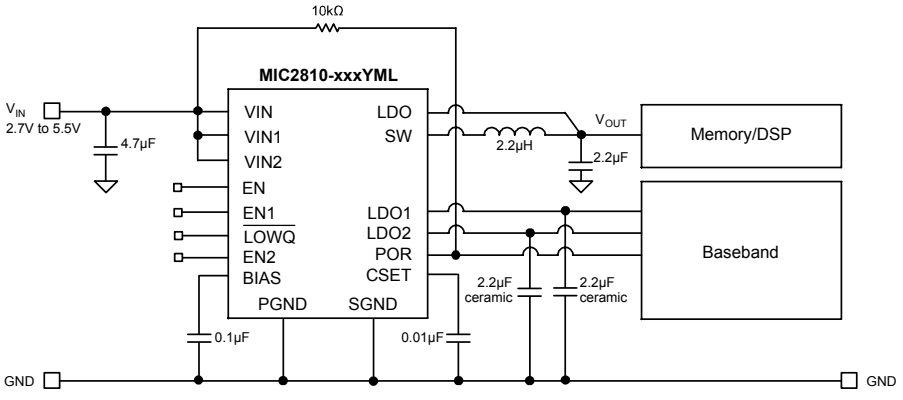
LDOs

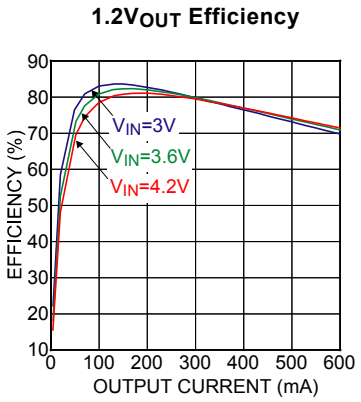
- LDO1
  - 1.65V to 5.5V input voltage range
  - 300mA Output current
  - Output voltage down to 0.8V
- LDO2
  - 2.7V to 5.5V input voltage range
  - 300mA Output current
  - Output voltage down to 0.8V

Applications

- Mobile phones
- PDAs
- GPS receivers
- Digital still cameras
- Portable media players

Typical Application





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MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology, Inc.

Ordering Information

Part number	Manufacturing Part Number	Voltage*	Junction Temperature Range	Package
MIC2810-1.2/1.2/2.8YML	MIC2810-44MYML	1.2V/1.2V/2.8V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2810-1.2/1.8/2.6YML	MIC2810-4GKYML	1.2V/1.8V/2.6V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2810-1.2/1.8/2.8YML	MIC2810-4GMYML	1.2V/1.8V/2.8V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2810-1.2/1.8/3.0YML	MIC2810-4GPYML	1.2V/1.8V/3.0V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2810-1.2/1.8/3.3YML	MIC2810-4GSYML	1.2V/1.8V/3.3V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2810-1.2/2.7/3.3YML	MIC2810-4LSYML	1.2V/2.7V/3.3V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2810-1.2/2.8/3.3YML	MIC2810-4MSYML	1.2V/2.8V/3.3V	–40°C to +125°C	16-Pin 3x3 MLF®

Notes:

Other voltage options available. Please contact Micrel for details.

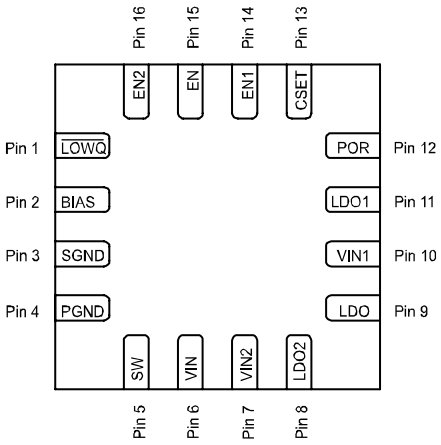
DC/DC – Fixed Output Voltages.

LDO1 – Output Voltage Range of 0.8V to 3.6V.

LDO2 – Output Voltage Range of 0.8V to 3.6V.

* Refers to nominal output voltage of DC/DC, LDO1, and LDO2 respectively.

Pin Configuration



16-Pin 3mm x 3mm MLF® (ML)

Pin Description

Pin Number	Pin Name	Pin Function
1	/LOWQ	LOWQ Mode. Active Low Input. Logic High = Full Power (Normal) Mode; Logic Low = LOWQ Mode; Do not leave floating.
2	BIAS	Internal circuit bias supply. It must be de-coupled to signal ground with a 0.1µF capacitor and should not be loaded.
3	SGND	Signal ground.
4	PGND	Power ground.
5	SW	Switch: Internal power MOSFET output switches.
6	VIN	Supply Input – DC/DC and other circuitry shared with LDO1 and LDO2. Must be connected to PIN 7.
7	VIN2	Supply Input – LDO2. Must be connected to PIN 6.
8	LDO2	Output of LDO2
9	LDO	LDO Output: Connect to V_{OUT} of the DC/DC for LOWQ mode operation.
10	VIN1	Supply Input – LDO1.
11	LDO1	Output of LDO1
12	POR	Power-On Reset Output: Open-drain output. Active low indicates an output undervoltage condition on either one of the three regulated outputs.
13	CSET	Delay Set Input: Connect external capacitor to GND to set the internal delay for the POR output. When left open, there is minimum delay. This pin cannot be grounded.
14	EN1	Enable Input (LDO 1). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating
15	EN	Enable Input (DC/DC). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating.
16	EN2	Enable Input (LDO 2). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}, V_{IN1}, V_{IN2})..... 0V to 6V
Enable Input Voltage (V_{EN}, V_{EN1}, V_{EN2})..... 0V to V_{IN}
Power Dissipation ..... Internally Limited[3]
Lead Temperature (soldering, 10 sec.)..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C
ESD Rating[4]..... 2kV

Operating Ratings[2]

Supply Voltage (V_{IN}, V_{IN2})..... 2.7V to 5.5V
Supply Voltage (V_{IN1})..... 1.65V to 5.5V
Enable Input Voltage (V_{EN}, V_{EN1}, V_{EN2})..... 0V to V_{IN}
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
MLF-16 (θ_{JA}) ..... 56°C/W

Electrical Characteristics[5]

$V_{IN} = V_{IN1} = V_{IN2} = EN1 = EN2 = EN = /LOWQ = V_{OUT}$[6] + 1V; $C_{OUTDC/DC} = 2.2\mu F$, $C_{LDO1} = C_{LDO2} = 2.2\mu F$; $I_{OUTDC/DC} = 100mA$; $I_{OUTLDO1} = I_{OUTLDO2} = 100\mu A$; $T_J = 25°C$, **bold** values indicate –40°C ≤ T_J ≤ +125°C; unless noted.

Parameter	Conditions	Min	Typ	Max	Units
UVLO Threshold	Rising input voltage during turn-on	**2.45**	2.55	**2.65**	V
UVLO Hysteresis			100		mV
Ground Pin Current	V_{FB} = GND (not switching);		800	1100	µA
	LDO1 or LDO2 (EN = GND; EN1 or EN2 = GND)		55	85 **95**	µA µA
Ground Pin Current in Shutdown	EN = EN1 = EN2 = 0V		0.2	5	µA
Ground Pin Current (LOWQ® mode)	$I_{DC/DC} \leq I_{LDO1} \leq I_{LDO2} \leq 10mA$ (/LOWQ = GND)		38	60 **80**	µA µA
	LDO1 or LDO2 (EN = GND; EN1 or EN2 = GND); $I_{OUT} \leq 10mA$ (/LOWQ = GND)		20	**70**	µA
Over-temperature Shutdown			160		°C
Over-temperature Shutdown Hysteresis			23		°C
Enable Inputs (EN; EN1; EN2; /LOWQ)					
Enable Input Voltage	Logic Low			**0.2**	V
	Logic High	**1.0**			V
Enable Input Current	$V_{IL} \leq 0.2V$		0.1	**1**	µA
	$V_{IH} \geq 1.0V$		0.1	**1**	µA
Turn-on Time					
Turn-on Time (LDO1 and LDO2)			240	**500**	µs
Turn-on Time (DC/DC)	(/LOWQ = V_{IN}; I_{LOAD} = 300mA); (/LOWQ = GND; I_{LOAD} = 10mA)		83	**350**	µs
POR Output					
VTH	Low Threshold, % of nominal ($V_{DC/DC}$ or V_{LDO1} or V_{LDO2}) (Flag ON)	90	91		%
	High Threshold, % of nominal ($V_{DC/DC}$ AND V_{LDO1} AND V_{LDO2}) (Flag OFF)		96	99	%
VOL	POR Output Logic Low Voltage; IL = 250µA		10	**100**	mV
IPOR	Flag Leakage Current, Flag OFF		0.01	**1**	µA
SET INPUT					
SET Pin Current Source	VSET = 0V	0.75	1.25	1.75	µA
SET Pin Threshold Voltage	POR = High		1.25		V

Electrical Characteristics - DC/DC Converter

$V_{IN} = V_{OUTDC/DC} + 1$; EN = V_{IN}; EN2 = EN1 = GND; $I_{OUTDC/DC}$ = 100mA ;L = 2.2µH; $C_{OUTDC/DC}$ = 2.2µF; T_J = 25°C,
bold values indicate –40°C to + 125°C; unless noted.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{\text{LOWQ}}$ = High (Full Power Mode)					
Fixed Output Voltages	Nominal V_{OUT} tolerance	–2 **–3**		+2 **+3**	% %
Output Voltage Line Regulation	V_{OUT} > 2.4V; V_{IN} = V_{OUT} + 300mV to 5.5V, I_{LOAD}= 100mA V_{OUT} < 2.4V; V_{IN} = 2.7V to 5.5V, I_{LOAD}= 100mA		0.2		%/V
Output Voltage Load Regulation	20mA < I_{LOAD} < 600mA		0.1		%
Maximum Duty Cycle	$V_{FB} \leq$ 0.4V	100			%
PWM Switch ON-Resistance	I_{SW} = 150mA V_{FB} = 0.7V_{FB_NOM} PMOS I_{SW} = -150mA V_{FB} = 1.1V_{FB_NOM} NMOS		0.5 0.6		Ω Ω
Oscillator Frequency		**1.8**	2	**2.2**	MHz
Current Limit in PWM Mode	V_{FB} = 0.9*V_{NOM}	0.75	1	1.6	A
$\overline{\text{LOWQ}}$ = Low (Light Load Mode)					
Output Voltage Accuracy	Variation from nominal V_{OUT}	–2		+2	%
	Variation from nominal V_{OUT}; –40°C to +125°C	**–3**		**+3**	%
Line Regulation	V_{IN} = V_{OUT} + 1V to 5.5V; I_{OUT} = 100µA		0.02	0.3 **0.6**	%/V %/V
Load Regulation	I_{OUT} = 100µA to 50mA		0.4	1.5	%
Ripple Rejection	f = up to 1kHz		45		dB
Current Limit	V_{OUT} = 0V	80	120	**220**	mA
Output Voltage Noise	10Hz to 100KHz		53		μV_{RMS}

Electrical Characteristics – LDO1/LDO2

$V_{IN1} = V_{IN2} = V_{OUTLDO1} + 1.0V$ or $V_{IN1} = V_{IN2} = V_{OUTLDO2} + 1.0V$; EN = GND; EN1 = EN2 = $V_{IN1} = V_{IN2}$; $C_{LDO1} = C_{LDO2} = 2.2\mu F$; $I_{OUTLDO1} = 100\mu A$; $T_J = 25°C$, **bold** values indicate $–40°C \leq T_J \leq +125°C$; unless noted.

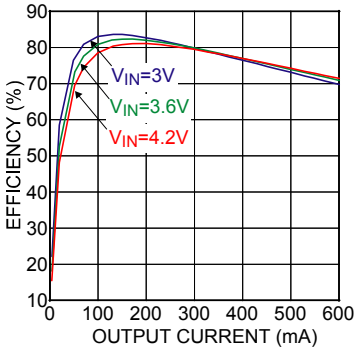
Parameter	Conditions	Min	Typ	Max	Units
$\overline{\text{LOWQ}}$ = High (Full Power Mode)					
Output Voltage Accuracy	Variation from nominal V_{OUT}	–2		+2	%
	Variation from nominal V_{OUT}; –40°C to +125°C	**–3**		**+3**	%
Line Regulation	$V_{IN} = V_{OUT}$ +1V to 5.5V		0.02	0.3 **0.6**	%/V
Load Regulation	I_{OUT} = 100µA to 150mA I_{OUT} = 100µA to 200mA I_{OUT} = 100µA to 300mA		0.20 0.25 0.40	 **1.5**	% % %
Dropout Voltage	I_{OUT} = 150mA I_{OUT} = 200mA I_{OUT} = 300mA		70 94 142	 **300**	mV mV mV
Ripple Rejection	f = up to 1kHz		35		dB
Current Limit	V_{OUT} = 0V	400	600	850	mA
Output Voltage Noise	10Hz to 100kHz		91		μV_{RMS}
$\overline{\text{LOWQ}}$ = Low (Light Load Mode)					
Output Voltage Accuracy	Variation from nominal V_{OUT}	–3		+3	%
	Variation from nominal V_{OUT}; –40°C to +125°C	**–4**		**+4**	%
Line Regulation	$V_{IN} = V_{OUT}$ +1V to 5.5V		0.02	0.3 **0.6**	%/V
Load Regulation	I_{OUT} = 100µA to 10mA		0.2	**1.0**	%
Dropout Voltage	I_{OUT} = 10mA		22	35 **50**	mV mV
Ripple Rejection	f = up to 1kHz		35		dB
Current Limit	V_{IN} = 2.7V; V_{OUT} = 0V	50	85	125	mA

Notes:

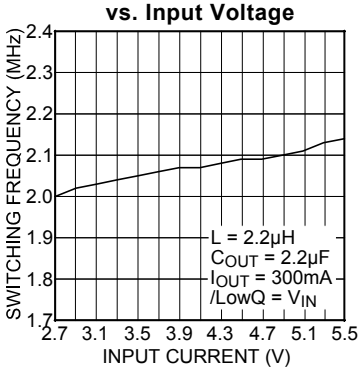
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
5. Specification for packaged product only.

Typical Characteristics — DC/DC Normal Mode (/LOWQ = VIN)

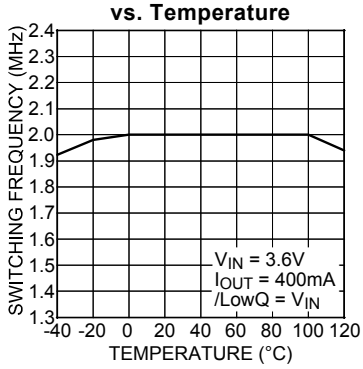
1.2V$_{OUT}$ Efficiency



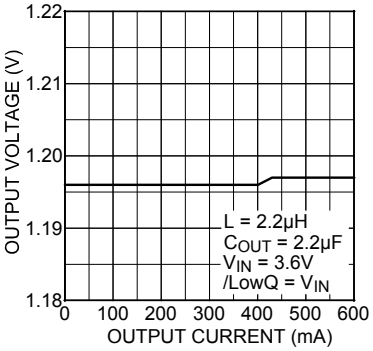
Switching Frequency vs. Input Voltage



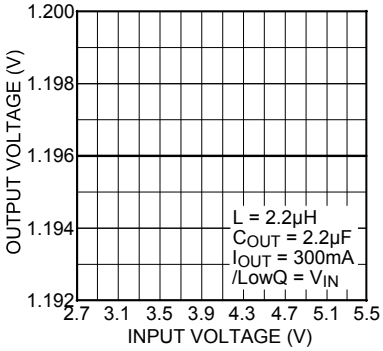
Switching Frequency vs. Temperature



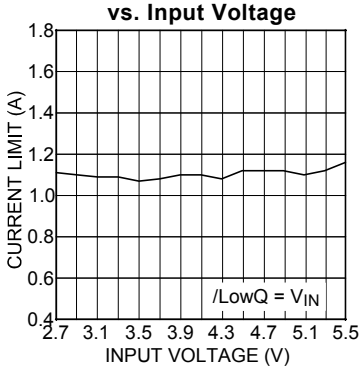
Load Regulation



Line Regulation

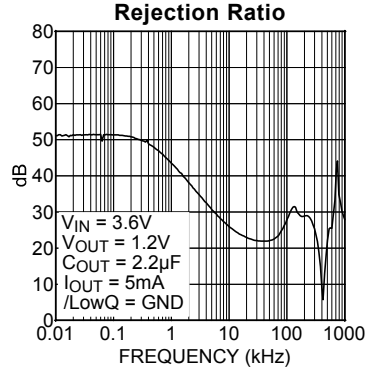


Current Limit vs. Input Voltage

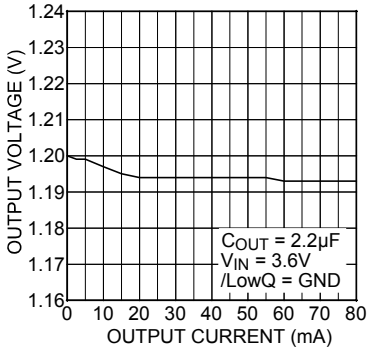


Typical Characteristics — DC/DC LOWQ Mode (/LOWQ = GND)

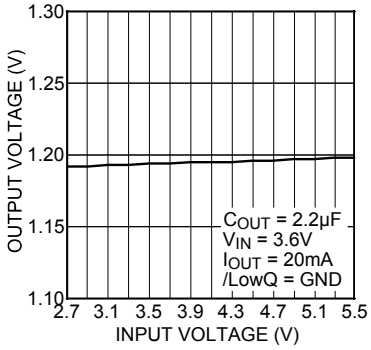
Power Supply Rejection Ratio



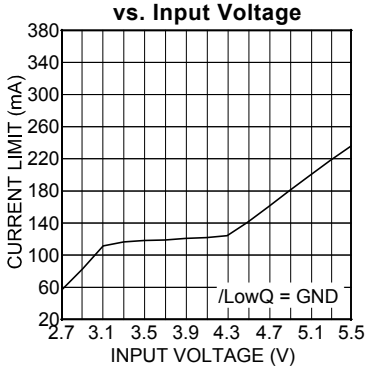
Load Regulation



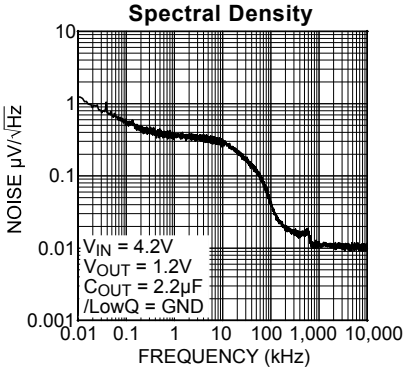
Line Regulation



Current Limit vs. Input Voltage

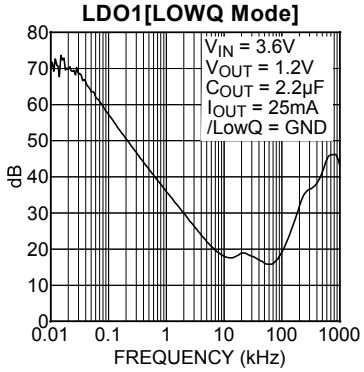


Output Noise Spectral Density

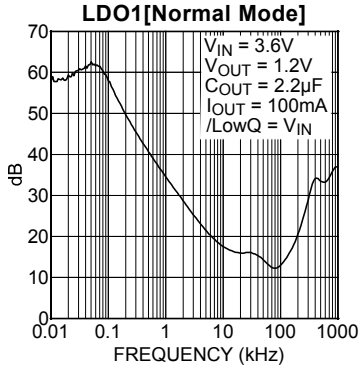


Typical Characteristics — LDO1/LDO2

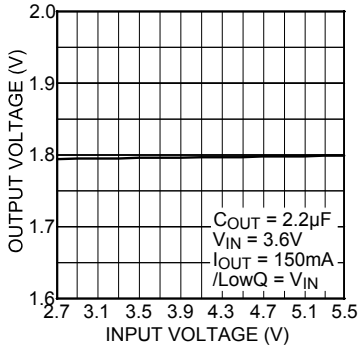
Power Supply Rejection Ratio LDO1[LOWQ Mode]



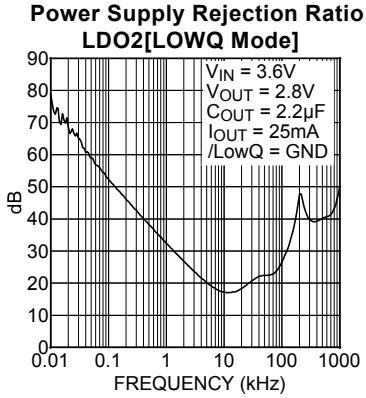
Power Supply Rejection Ratio LDO1[Normal Mode]



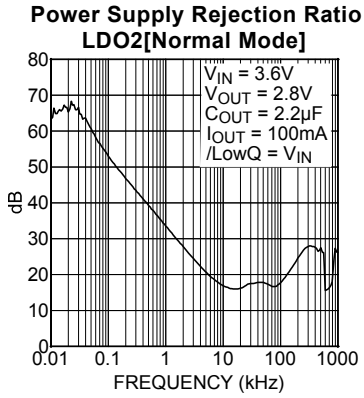
LDO1 Line Regulation



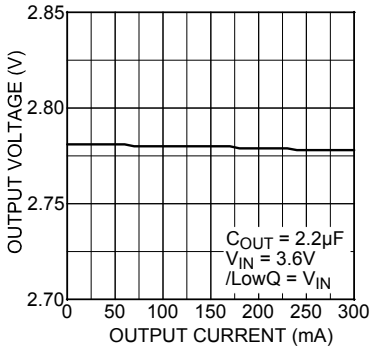
Power Supply Rejection Ratio LDO2[LOWQ Mode]



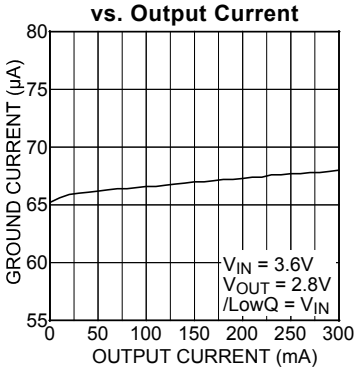
Power Supply Rejection Ratio LDO2[Normal Mode]



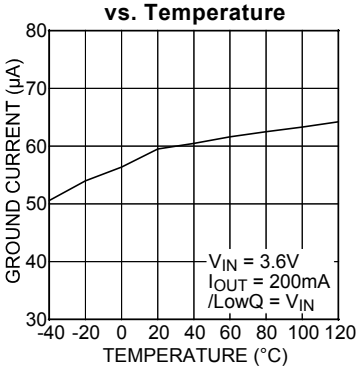
LDO2 Load Regulation



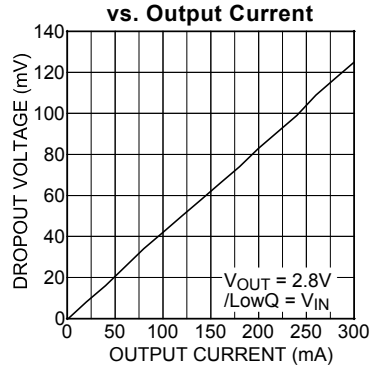
LDO2 Ground Current vs. Output Current



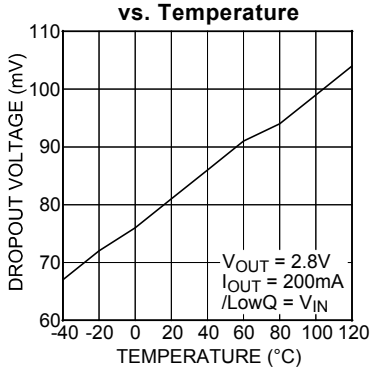
LDO2 Ground Current vs. Temperature



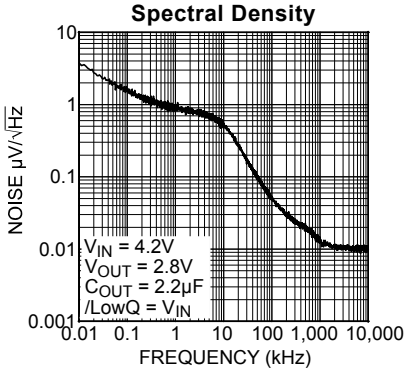
LDO2 Dropout Voltage vs. Output Current



LDO2 Dropout Voltage vs. Temperature

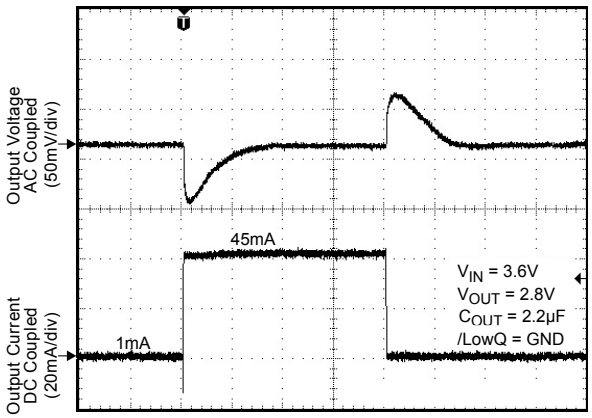


LDO2 Output Noise Spectral Density

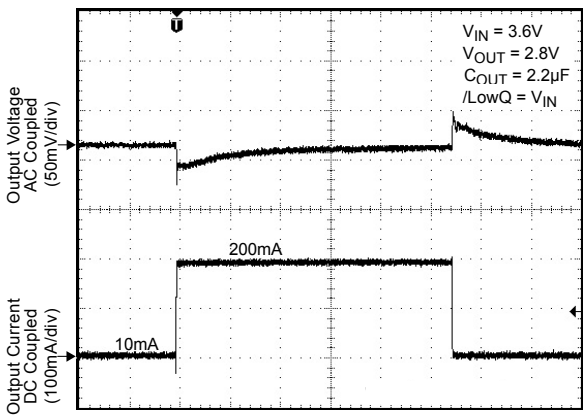


Functional Characteristics

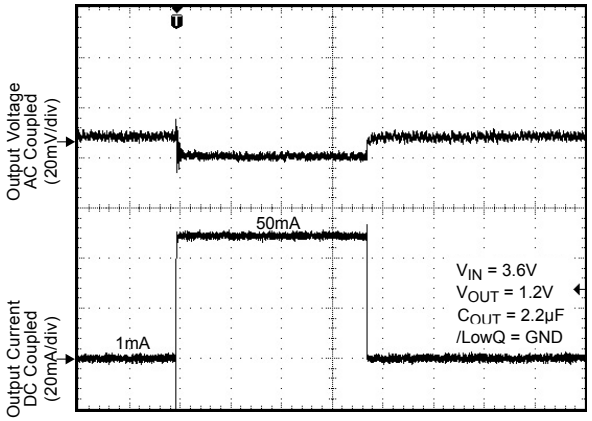
LDO2[LOWQ Mode] Load Transient



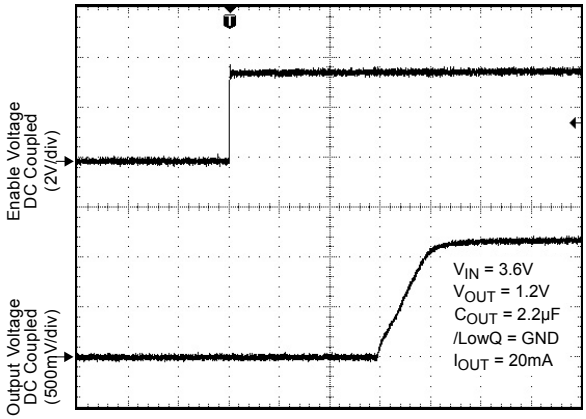
LDO2[Normal Mode] Load Transient



DC/DC[LOWQ Mode] Load Transient

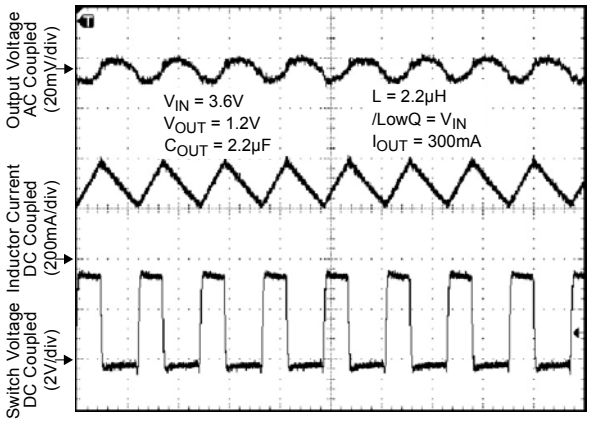


DC/DC[LOWQ Mode] Start-Up Waveforms

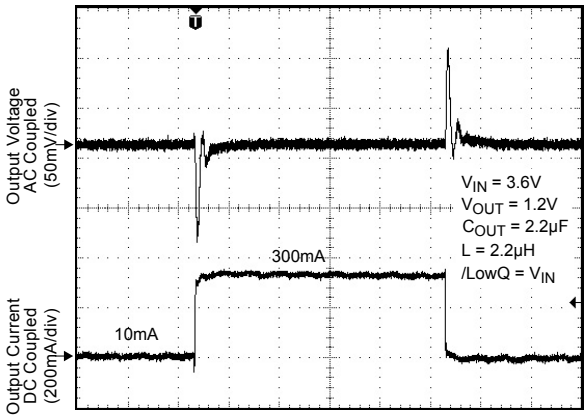


Functional Characteristics (cont.)

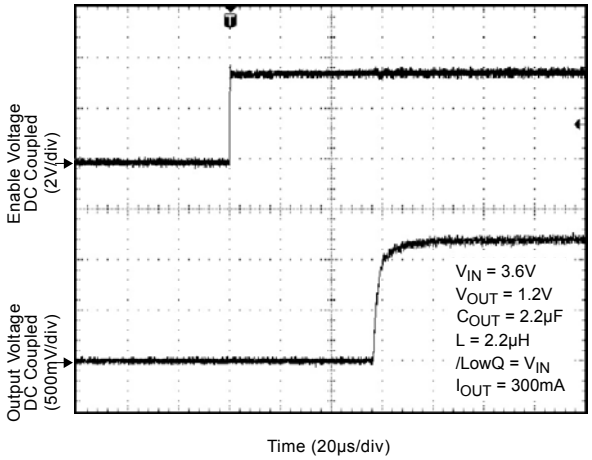
DC/DC PWM Waveforms



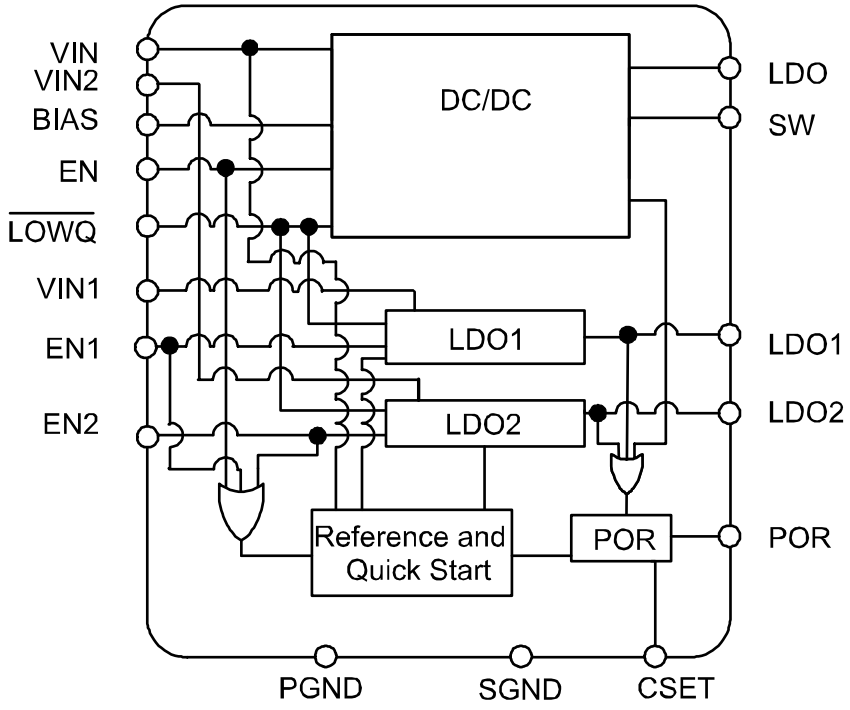
DC/DC Load Transient



DC/DC Start-Up Waveforms



Functional Diagram



MIC2810 Block Diagram

Device Functional Description

The MIC2810 is a power management IC with a single integrated step-down regulator and two low dropout regulators. LDO1 and LDO2 are 300mA low dropout regulators supplied from the input voltage pins. The step-down regulator is a 600mA PWM power supply. All three regulators utilize a /LOWQ light load mode to maximize battery efficiency under light load conditions. This is achieved with a /LOWQ control pin that when pulled low shuts down all the biasing and drive current for the PWM regulator, along with reducing the current limit of the two independent LDOs. When the /LOWQ pin is pulled low, the MIC2810 draws only 30µA of operating current. This mode allows the output to be regulated through the LDO output which is capable of providing 60mA of output current. This method has the advantage of producing a clean, low current, ultra-low noise output in /LOWQ mode. During /LOWQ mode, the SW node becomes high impedance, blocking current flow. Other methods of reducing quiescent current, such as pulse frequency modulation (PFM) or bursting techniques create large amplitude and low frequency ripple voltages that can be detrimental to system operation.

When more than 60mA is required, the /LOWQ pin can be forced high, causing the MIC2810 to enter PWM mode. In this case, the LDO output makes a "hand-off" to the PWM regulator with virtually no variation in output voltage. The LDO output then turns off allowing up to 600mA of current to be efficiently supplied through the PWM output to the load.

Pin Functional Description

VIN/VIN1/VIN2

Three input voltage pins provide power to the switch mode regulator, LDO1, and LDO2. VIN provides power to the control circuitry of the DC/DC converter and voltage reference circuitry shared by all the regulators in the MIC2810. LDO1's input voltage (VIN1) can go down to 1.65V but LDO2 and the DC/DC converter input voltages are limited to 2.7V minimum.

For the switch mode regulator VIN provides power to the MOSFET along with current limiting sense circuitry. Due to the high switching speeds, a 4.7µF capacitor is recommended close to VIN and the power ground (PGND) pin for bypassing. Please refer to the PCB layout section for an example of an appropriate circuit layout.

LDO

The LDO pin is the output of the linear regulator and should be connected to the output of the step-down PWM regulator. In /LOWQ mode (/LOWQ <0.2V), the LDO provides the output voltage of the DC/DC regulator.

LDO1

Regulated output voltage of LDO1. Power is provided by VIN1. Recommended output capacitance is 2.2µF.

LDO2

Regulated output voltage of LDO2. Power is provided by VIN2. Recommended output capacitance is 2.2µF.

EN/EN1/EN2

All enable inputs are active high, requiring 1.0V for guaranteed operation. EN provides logic control for the DC/DC regulator. EN2 provides logic control for LDO2, and EN1 provides logic control for LDO1. The enable inputs are CMOS logic and cannot be left floating.

The enable pins provide logic level control of the specified outputs. When all enable pins are in the off state, supply current of the device is greatly reduced (typically <1µA). When the DC/DC regulator is in the off state, the output drive is placed in a "tri-stated" condition, where both the high side P-channel MOSFET and the low-side N-channel are in an "off" or non-conducting state. Do not drive any of the enable pins above the supply voltage.

Power-On Reset (POR)

The power-on reset output is an open-drain N-Channel device, requiring a pull-up resistor to either the input voltage or output voltage for proper voltage levels. The POR output has a delay time that is programmable with a capacitor from the CSET pin to ground. The delay time can be programmed to be as long as 1 second.

/LOWQ

The /LOWQ pin provides a logic level control between the internal PWM switching regulator mode, and the low noise linear regulator mode. With /LOWQ pulled low (≤0.2V), quiescent current of the device is greatly reduced by switching to a low noise linear regulator mode that has a typical supply current of 38µA. In linear (LDO) mode the output can deliver 60mA of current to the output. By placing /LOWQ high (≥1V), the device transitions into a constant frequency PWM step-down regulator mode. This allows the device the ability to efficiently deliver up to 600mA of output current at the same output voltage.

/LOWQ mode also limits the output load of both LDO1 and LDO2 to <50mA.

BIAS

The BIAS pin supplies the power to the internal control and reference circuitry. The bias is powered from VIN through an internal 6Ω resistor. A small 0.1µF capacitor is recommended for bypassing.

SW

The switch (SW) pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

PGND

Power ground (PGND) is the ground path for the high current PWM mode. The current loop for the power ground should be as small as possible.

SGND

Signal ground (SGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be as small as possible.

CSET

The CSET pin is a current source output that charges a capacitor that sets the delay time for the power-on reset output from low to high. The delay for POR high to low (detecting an undervoltage on any of the outputs) is always minimal. The current source of 1.25µA charges a capacitor up from 0V. When the capacitor reaches 1.25V, the output of the POR is allowed to go high. The delay time in microseconds is equal to the Cset in picofarads.

POR Delay (µs) = CSET (pF)

Component Selection

Output Capacitor

LDO1 and LDO2 outputs require a 2.2µF ceramic output capacitor for stability. The DC/DC switch mode regulator also requires a 2.2µF ceramic output capacitor to be stable. All output capacitor values can be increased to improve transient response, but performance has been optimized for a 2.2µF ceramic on the LDOs and the DC/DC regulator. X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X5R/X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% to 60% respectively over their operating temperature ranges.

Input Capacitor

A minimum 1µF ceramic, 4.7µF recommended, should be placed as close as possible to the VIN pin for optimal bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended. A minimum 1µF is recommended close to the VIN and PGND pins for high frequency filtering. Smaller case size capacitors are recommended due to their lower ESR and ESL. Please refer to the PCB layout section for an example of an appropriate circuit layout.

Inductor Selection

The MIC2810 is designed for use with a 2.2µH inductor. Proper selection should ensure the inductor can handle the maximum average and peak currents required by the load. Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure that the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. Peak inductor current can be calculated as follows:

$$I_{PK} = I_{OUT} + \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2 \times f \times L}$$

I_{PK}: Peak Inductor Current

I_{OUT}: Output/Load Current

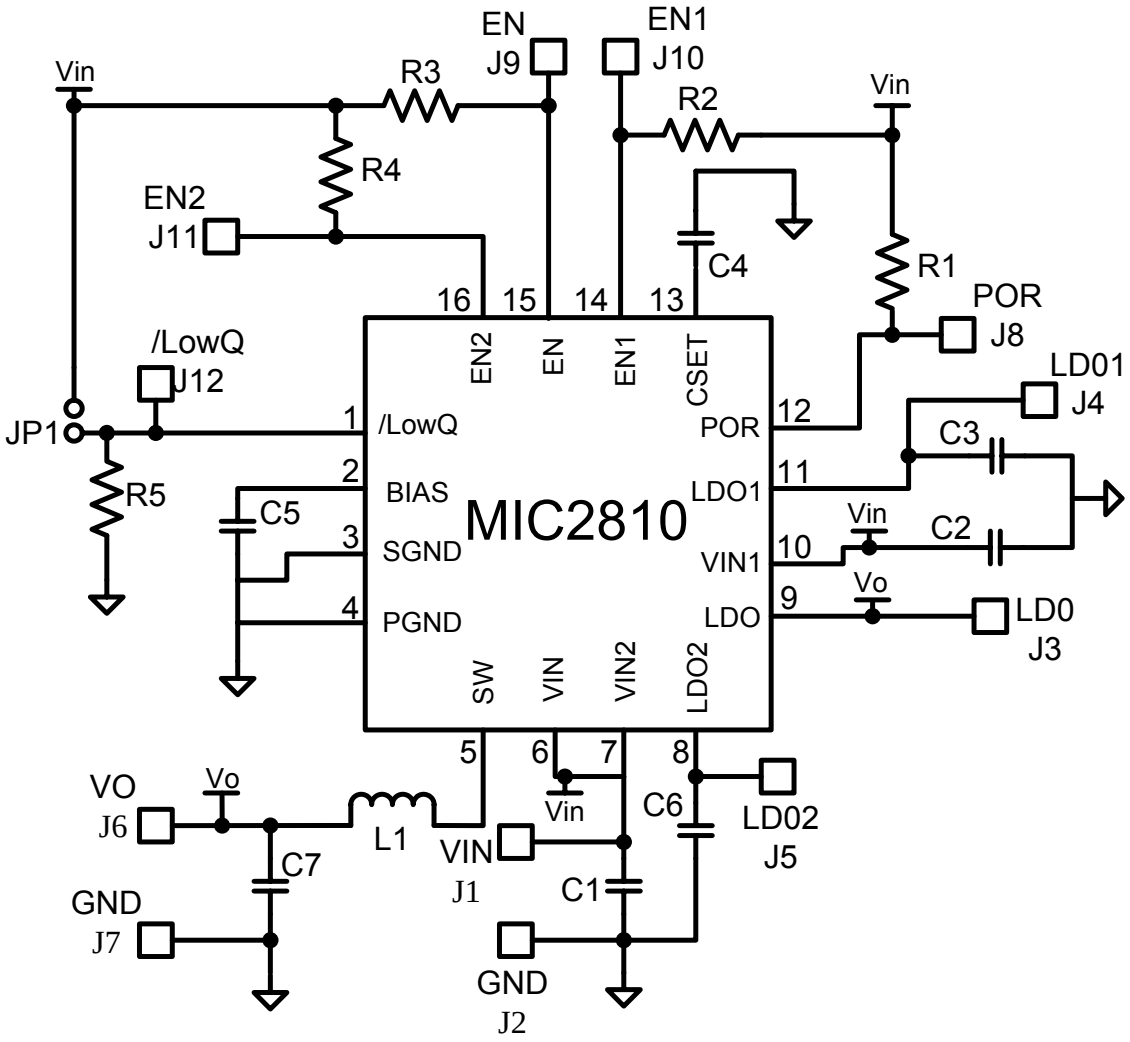
V_{IN}: Input Voltage

V_{OUT}: Output Voltage

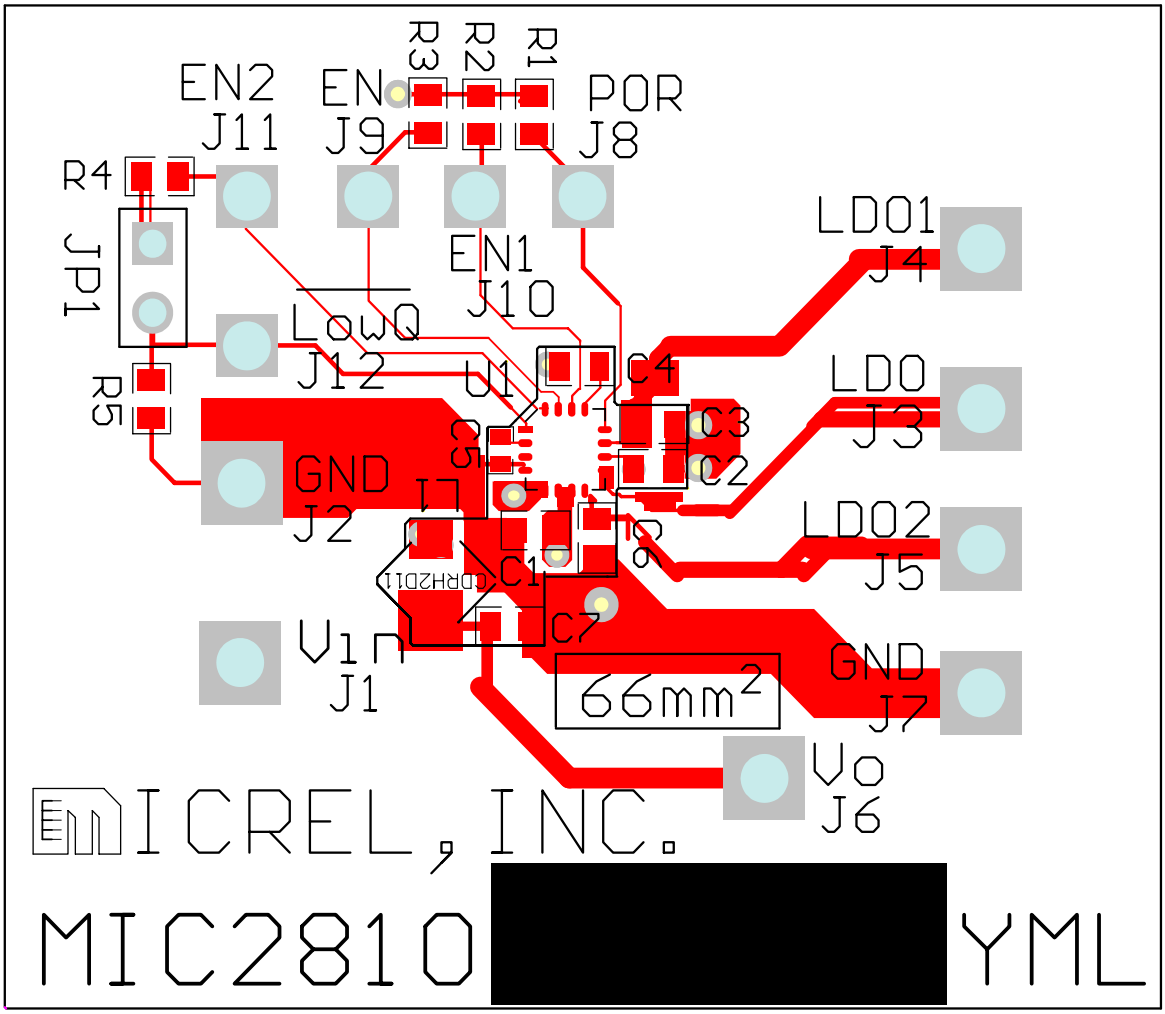
f: Switching Frequency of PWM Regulator

L: Inductor Value

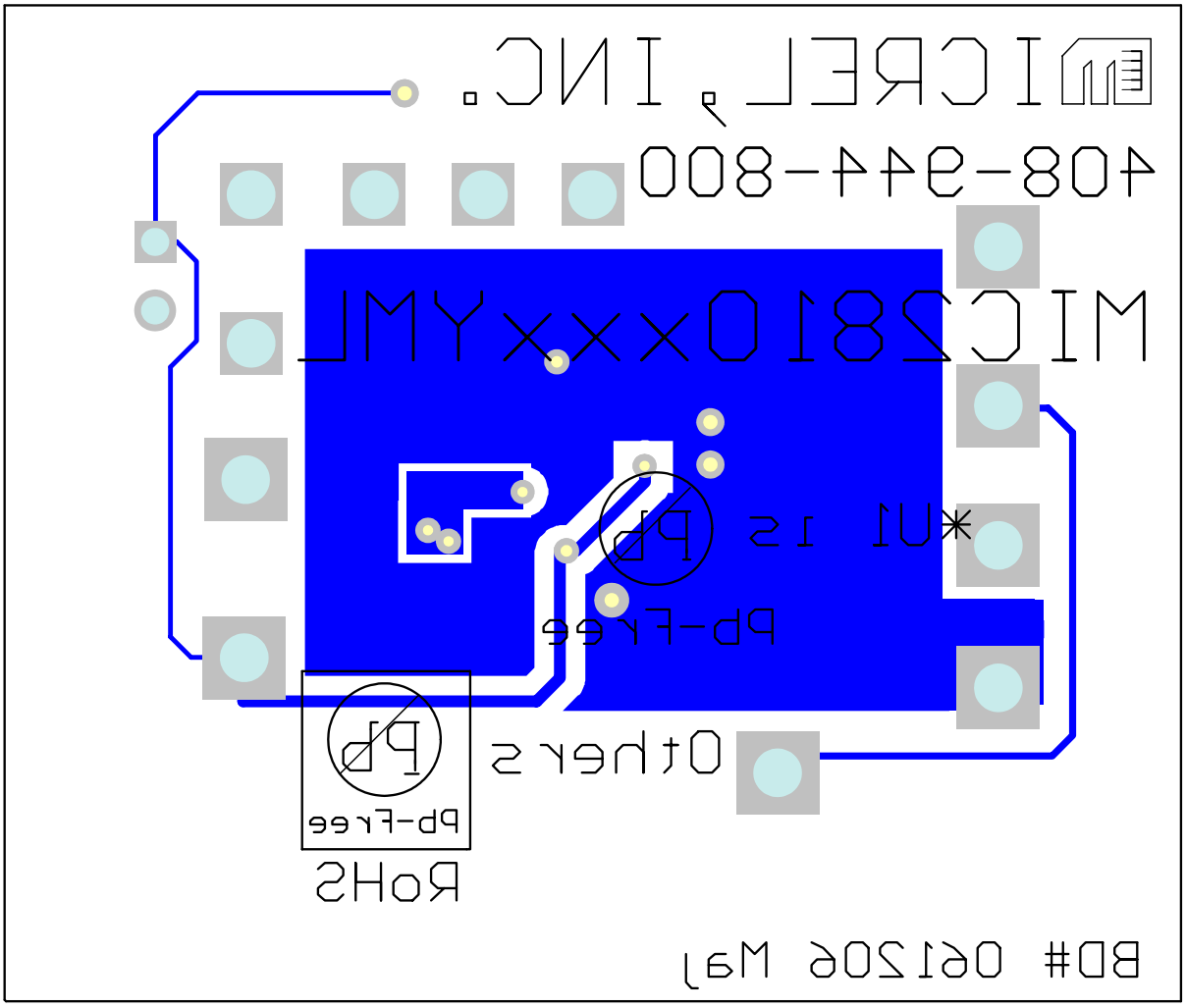
PCB Layout



Layout Schematic

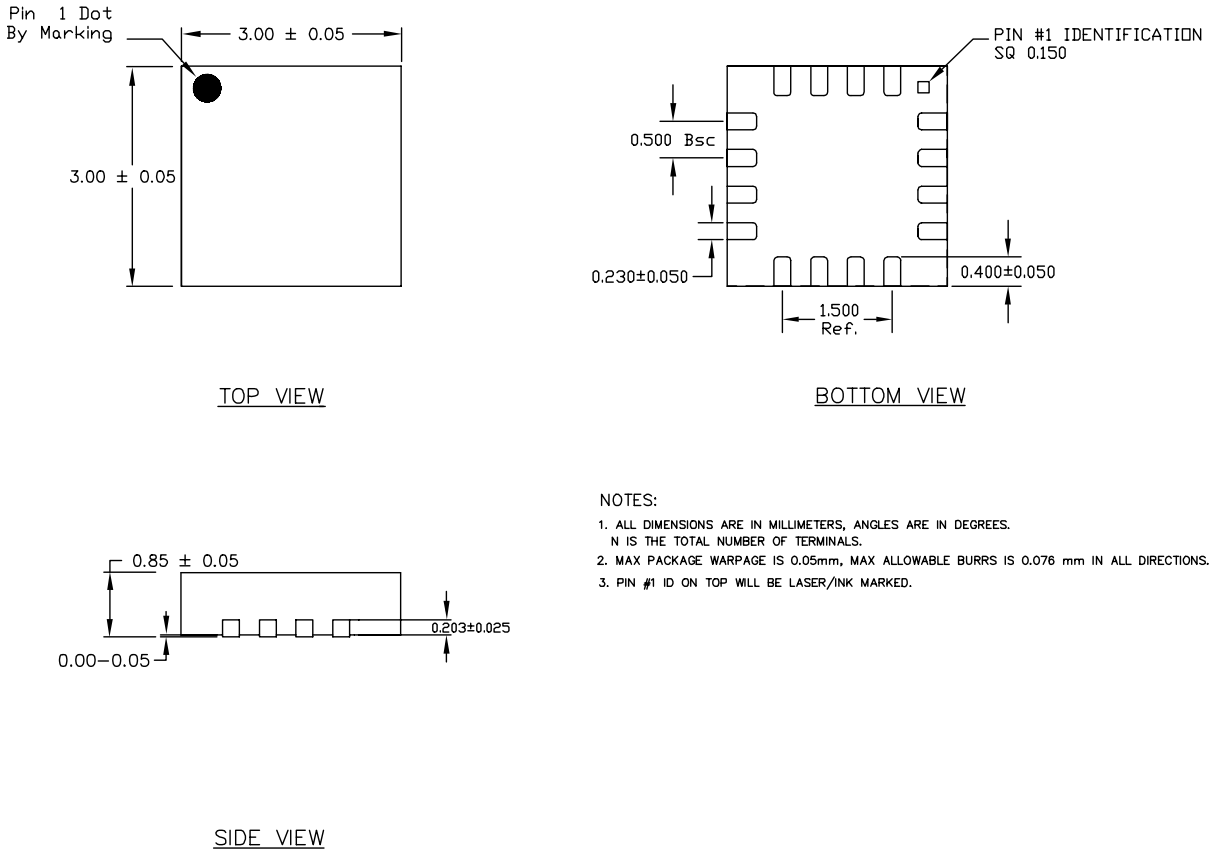

R3
R2
R1
EN2
J11
EN
J9
POR
J8
R4
JP1
R5
EN1
J10
LDO1
J4
LOWQ
J12
U1
C4
LDO
J3
C3
C2
C5
GND
J2
LDO2
J5
C1
C7
VIN
J1
66mm²
GND
J7
VO
J6
MICREL, INC.
MIC2810
YML

Top Layer



Bottom Layer

Package Information



16-Pin 3mm x 3mm MLF® (ML)

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